Abstract of the Disclosure

A digital base booster (DBB) for reducing hardware by using an arithmetic processor is provided. Instead of using a conventional IIR filter having a cascade structure including a plurality of partial building blocks, the digital base booster using an arithmetic processor includes first internal data, an inputting portion, a data assigner, an arithmetic portion, and an output data storing device. The first internal data is the output data of the arithmetic portion. The inputting portion includes a plurality of multi-bit registers, thereby storing input data and the first internal data and outputting the stored data in a predetermined signal. The data assigner selects one output data from a plurality of output data of the inputting portion. The arithmetic portion performs an arithmetic operation on the output data of the data assigner and data stored in the arithmetic portion, compensates for and stores a round-off error of the data output by the operation, and outputs the first internal data. The output data storing device stores and outputs data processed in the arithmetic portion.

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